WHAT IS CLAIMED IS:

1. A semiconductor device comprising a semiconductor substrate having an active region, and a device isolation region that defines the active region on the substrate, and wherein the active region includes a central part, end parts, and connection parts extending along a first axis from the central part to the end parts, respectively, so as to connect the central part to the end parts, the connection parts each having a width that is less than each of the maximum widths of the central part and the end parts as measured in the direction of a second axis perpendicular to said first axis.

2. The device of claim 1, wherein the maximum width of the central part of the active region is greater than the maximum width of each of the end parts as measured in the direction of said second axis.

3. The device of claim 1, and further comprising gate electrodes that extend across the connection parts of the active region, respectively, in the direction of said second axis.

4. The device of claim 3, and further comprising a bit line electrically connected to the central part of the active region, and a capacitor electrically connected to a said end part of the active region.

5. The device of claim 4, wherein the capacitor is located over the bit line.

6. The device of claim 1, wherein said substrate has a trench therein, and a layer of insulation material fills said trench and constitutes said device isolation region.

7. The device of clam 6, wherein said central and end parts of the active region are portions of said substrate doped with impurity ions.

8. The device of clam 1, wherein said central and end parts of the active region are portions of said substrate doped with impurity ions.

9. A semiconductor device comprising a semiconductor substrate having an active region, a device isolation region that defines the active region on the substrate, and gate electrodes spaced from one another in the direction of a first axis,

the active region having a width that varies along the direction of the first axis, said width being the dimension of the active region measured in the direction of a second axis perpendicular to said first axis, and

the gate electrodes extending in the direction of said second axis across the device isolation region and across the portions of the gate electrodes having the smallest width measured in the direction of said second axis.

10. The device of claim 9, wherein a pair of said gate electrodes extends across the active region, the active region having an active region central part located between the pair of gate electrodes, active region end parts, and active region channel parts disposed between the active region central part and the active region end parts, respectively, the gate electrodes extending across the active region channel parts, and the width of the active region at said central part thereof being greater than the width of the active region at said end parts thereof.

11. The device of claim 10, and further comprising a bit line electrically connected to the active region central part, and a capacitor electrically connected to a said active region end part.

12. The device of claim 11, wherein the capacitor is located over the bit line.

13. The device of claim 9, wherein said substrate has a trench therein, and a layer of insulation material fills said trench and constitutes said device isolation region.

14. The device of clam 13, wherein said central and end parts of the active region are portions of said substrate doped with impurity ions.

15. The device of clam 9, wherein said central and end parts of the active region are portions of said substrate doped with impurity ions.